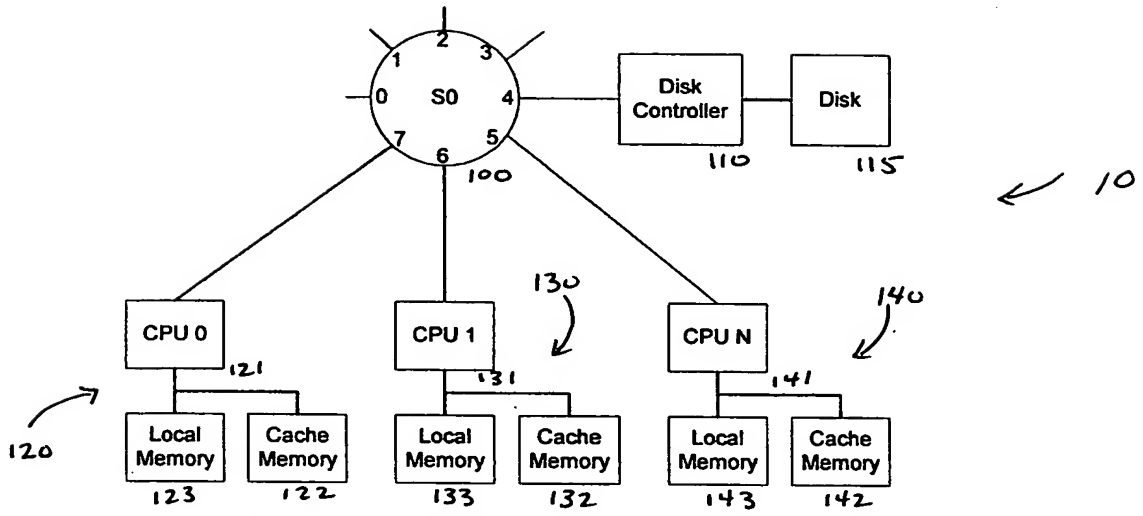

Figure 1. A distributed system with a single switch using shared memory

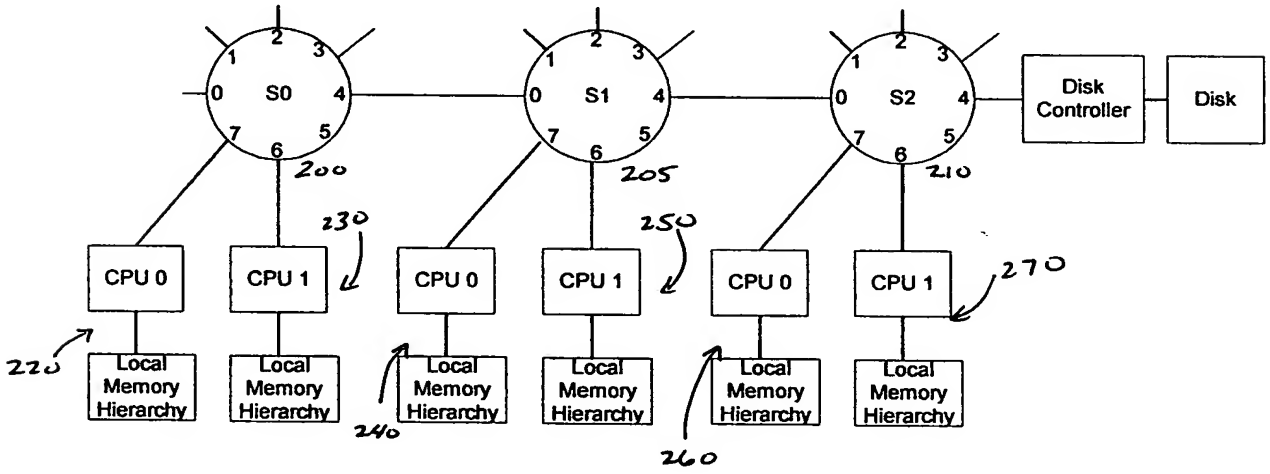

Figure 2. A distributed system with multiple switches using shared memory

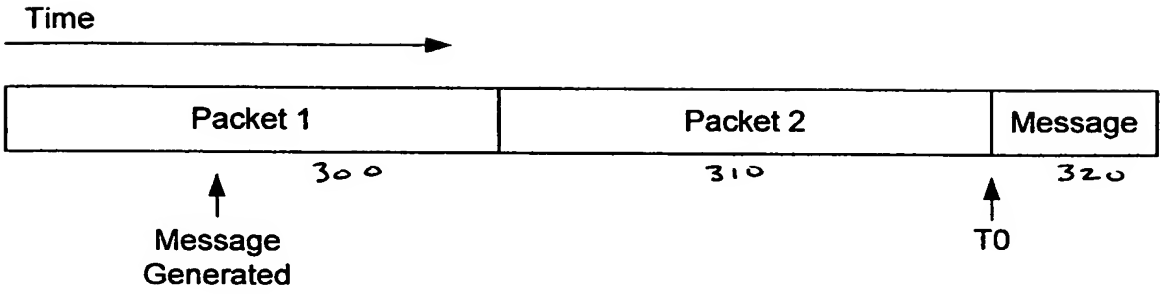

Figure 3a. Message inserted at tail of queue.

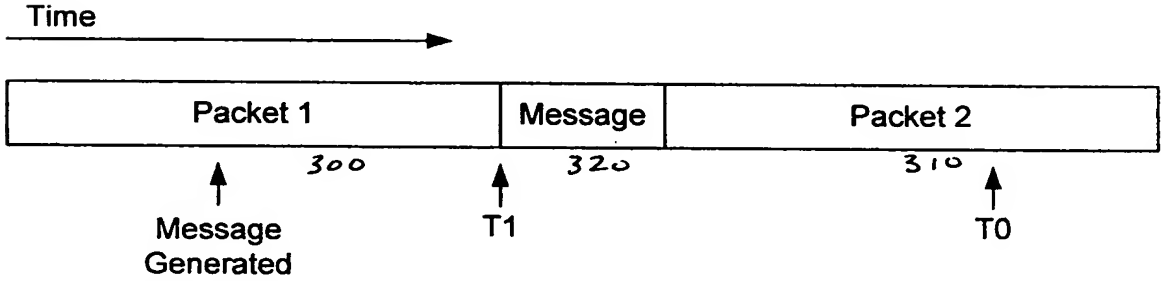

Figure 3b. Message inserted when packet in transmission is completed. Speed-up over Figure 3a is T0 – T1.

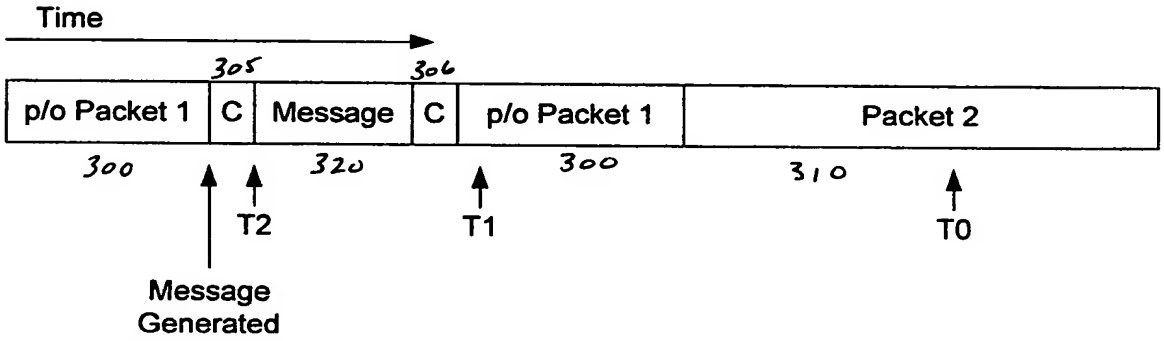

Figure 3c. Message inserted at earliest possible moment. Speed-up over Figure 3a is T0 – T2. Speed-up over Figure 3b is T1 – T2.

Cache Line	CPU 120	CPU 130	CPU 140
xxxxxxx	I	I	E
yyyyyyy	S	S	I
zzzzzzzz	O	S	I

Figure 4. Representative Directory Structure

Action	Switch 100 CPU 120	Switch 100 CPU 130	Switch 100 CPU 140
120 reads memory	E	I	I
130 reads	S	S	I
140 reads	S	S	S
130 modifies	I	M	I
140 reads	I	O	S
140 modifies	I	I	M

Figure 5. Directory Entries for Switch 100

Action	S200 P0	S200 P7	S200 P6	S200 P4	S205 P0	P205 P7	S205 P6	S205 P4	S210 P0	S210 P7	S210 P6	S210 P4
220 reads memory	I	E	I	I	E	I	I	I	I	I	I	I
230 reads	I	S	S	I	E	I	I	I	I	I	I	I
270 reads	I	S	S	I	S	I	I	S	S	I	S	I
270 modifies	I	I	I	M	I	I	I	M	I	I	M	I
250 reads	I	I	I	M	I	I	S	O	S	I	O	I
240 reads	I	I	I	M	I	S	S	O	S	I	O	I
240 modifies	I	I	I	M	I	M	I	I	M	I	I	I
230 reads	I	I	S	O	S	O	I	I	M	I	I	I

Figure 6. Directory Entries for Switches 200, 205 and 210